IN THE CLAIMS:

Please amend claims 1-3, 5, 6, 10-14, and 18-22, and add new claims 25 and 26 as follows:

1. (Currently Amended) An arithmetic circuit with built-in self testing of input-to-output delay for use with a Residue Number System (RNS), said arithmetic circuit comprising:

an arithmetic core for performing an RNS arithmetic operation, the arithmetic core having an output and at least two inputs;

input-to-output delay test circuitry coupled to the arithmetic core, the input-to-output delay test circuitry selectively feeding the output of the arithmetic core back to at least one of the inputs without latching so as to induce natural oscillation at the output of the arithmetic core during testing of the input-to-output delay; and

input-to-output delay logic circuitry coupled to the output of the arithmetic core, the input-to-output delay logic circuitry measuring an oscillation frequency of the output of the arithmetic core during testing of the input-to-output delay, making a determination of whether the oscillation frequency that is measured is at least equal to a minimum threshold value, and producing a ~~pass/fail~~ pass signal or a fail signal based on the determination that is made in order to indicate whether or not the input-to-output delay of the arithmetic core is within specification ~~based on a determination of whether the oscillation frequency is at least equal to a minimum threshold value~~.

2. (Currently Amended) The arithmetic circuit as defined in claim 1, wherein the input-to-output delay logic circuitry includes:

a counter coupled to the output of the arithmetic core, the counter counting oscillations of the output of the arithmetic core during testing of the input-to-output delay; and

a comparator coupled to the counter, the comparator comparing the output of the counter after a predetermined test period with the minimum threshold value and producing the ~~pass/fail~~ pass or fail signal.

3. (Currently Amended) The arithmetic circuit as defined in claim 2, wherein the input-to-output delay test circuitry includes:

a plurality of isolation buffers for isolating the inputs ~~and output~~ of the arithmetic core from upstream ~~and downstream~~ circuitry and the output of the arithmetic core from downstream circuitry during testing of the input-to-output delay; and

at least one transmission gate for ~~selectively~~ feeding the output of the arithmetic core back to one of the inputs of the arithmetic core without latching during testing of the input-to-output delay.

4. (Original) The arithmetic circuit as defined in claim 3, wherein the isolation buffers, the transmission gate, and the counter are controlled by a test enable signal.

5. (Currently Amended) The arithmetic circuit as defined in claim 1, wherein the input-to-output delay test circuitry includes:

a plurality of isolation buffers for isolating the inputs ~~and output~~ of the arithmetic core from upstream ~~and downstream~~ circuitry and the output of the arithmetic core from downstream circuitry during testing of the input-to-output delay; and

at least one transmission gate for ~~selectively~~ feeding the output of the arithmetic core back to one of the inputs of the arithmetic core without latching during testing of the input-to-output delay.

6. (Currently Amended) The arithmetic circuit as defined in claim 1, wherein the input-to-output delay test circuitry includes:

a plurality of isolation buffers for isolating the inputs ~~and output~~ of the arithmetic core from upstream ~~and downstream~~ circuitry and the output of the arithmetic core from downstream circuitry during testing of the input-to-output delay;

a first transmission gate for ~~selectively~~ feeding the output of the arithmetic core back to one of the inputs of the arithmetic core without latching during testing of the input-to-output delay; and

a second transmission gate for ~~selectively~~ supplying a constant to the other input of the arithmetic core during testing of the input-to-output delay.

7. (Original) The arithmetic circuit as defined in claim 6, wherein the isolation buffers and the transmission gates are controlled by a test enable signal.

8. (Previously Presented) The arithmetic circuit as defined in claim 1, wherein the arithmetic core is a One-Hot Residue Number System (OHRNS) modulo m adder.

9. (Previously Presented) The arithmetic circuit as defined in claim 1, wherein the arithmetic core is a One-Hot Residue Number System (OHRNS) modulo m multiplier.

10. (Currently Amended) A digital signal processing device having at least one Residue Number System (RNS) arithmetic circuit with built-in self testing of input-to-output delay, said arithmetic circuit comprising:

an arithmetic core for performing an RNS arithmetic operation, the arithmetic core having an output and at least two inputs;

input-to-output delay test circuitry coupled to the arithmetic core, the input-to-output delay test circuitry selectively feeding the output of the arithmetic core back to at least one of the inputs without latching so as to induce natural oscillation at the output of the arithmetic core during testing of the input-to-output delay; and

input-to-output delay logic circuitry coupled to the output of the arithmetic core, the input-to-output delay logic circuitry measuring an oscillation frequency of the output of the arithmetic core during testing of the input-to-output delay, making a determination of whether the oscillation frequency that is measured is at least equal to a minimum threshold value, and producing a ~~pass/fail~~ pass signal or a fail signal based on the determination that is made in order to indicate whether or not the input-to-output delay of the arithmetic core is within specification ~~based on a determination of whether the oscillation frequency is at least equal to a minimum threshold value~~.

11. (Currently Amended) The digital signal processing device as defined in claim 10, wherein the input-to-output delay logic circuitry of the arithmetic circuit includes:

a counter coupled to the output of the arithmetic core, the counter counting oscillations of the output of the arithmetic core during testing of the input-to-output delay; and

a comparator coupled to the counter, the comparator comparing the output of the counter after a predetermined test period with the minimum threshold value and producing the ~~pass/fail~~ pass or fail signal.

12. (Currently Amended) The digital signal processing device as defined in claim 11, wherein the input-to-output delay test circuitry of the arithmetic circuit includes:

a plurality of isolation buffers for isolating the inputs ~~and output~~ of the arithmetic core from upstream ~~and downstream~~ circuitry and the output of the arithmetic core from downstream circuitry during testing of the input-to-output delay; and

at least one transmission gate for ~~selectively~~ feeding the output of the arithmetic core back to one of the inputs of the arithmetic core without latching during testing of the input-to-output delay.

13. (Currently Amended) The digital signal processing device as defined in claim 10, wherein the input-to-output delay test circuitry of the arithmetic circuit includes:

a plurality of isolation buffers for isolating the inputs ~~and output~~ of the arithmetic core from upstream ~~and downstream~~ circuitry and the output of the arithmetic core from downstream circuitry during testing of the input-to-output delay; and

at least one transmission gate for ~~selectively~~ feeding the output of the arithmetic core back to one of the inputs of the arithmetic core without latching during testing of the input-to-output delay.

14. (Currently Amended) The digital signal processing device as defined in claim 10, wherein the input-to-output delay test circuitry of the arithmetic circuit includes:

a plurality of isolation buffers for isolating the inputs ~~and output~~ of the arithmetic core from upstream ~~and downstream~~ circuitry and the output of the arithmetic core from downstream circuitry during testing of the input-to-output delay;

a first transmission gate for ~~selectively~~ feeding the output of the arithmetic core back to one of the inputs of the arithmetic core without latching during testing of the input-to-output delay; and

a second transmission gate for ~~selectively~~ supplying a constant to the other input of the arithmetic core during testing of the input-to-output delay.

15. (Original) The digital signal processing device as defined in claim 14, wherein the isolation buffers and the transmission gates are controlled by a test enable signal.

16. (Previously Presented) The digital signal processing device as defined in claim 10, wherein the arithmetic core of the arithmetic circuit is a One-Hot Residue Number System (OHRNS) modulo m adder.

17. (Previously Presented) The digital signal processing device as defined in claim 10, wherein the arithmetic core of the arithmetic circuit is a One-Hot Residue Number System (OHRNS) modulo m multiplier.

18. (Currently Amended) A method for testing propagation delay of a Residue Number System (RNS) arithmetic circuit incorporated into an integrated circuit device, the arithmetic circuit including an arithmetic core that performs an RNS arithmetic operation, said method comprising the steps of:

selectively feeding the output of the arithmetic core back to one of the inputs of the arithmetic core without latching and selectively providing a constant to another input of the arithmetic core, so as to induce natural oscillation at the output of the arithmetic core during testing of the propagation delay;

measuring an oscillation frequency of the output of the arithmetic core during testing of the propagation delay;

making a determination of whether the oscillation frequency that is measured is at least equal to a minimum threshold value; and

producing a ~~pass/fail~~ pass signal or a fail signal based on the determination that is made in order to indicate whether or not the propagation delay of the arithmetic core is within specification ~~based on a determination of whether the oscillation frequency is at least equal to a minimum threshold value~~.

19. (Currently Amended) The method as defined in claim 18,

wherein the measuring step includes the sub-step of counting oscillations of the output of the arithmetic core during a predetermined time period, and

the ~~producing~~ making step includes the sub-step of comparing the counted oscillations with the minimum threshold value to ~~determine a pass or fail condition~~ make the determination.

20. (Currently Amended) The method as defined in claim 19, further comprising the step of isolating the inputs ~~and output~~ of the arithmetic core from upstream ~~and downstream~~ circuitry and the output of the arithmetic core from downstream circuitry during testing of the propagation delay.

21. (Currently Amended) The method as defined in claim 18, further comprising the step of isolating the inputs ~~and output~~ of the arithmetic core from upstream ~~and downstream~~ circuitry and the output of the arithmetic core from downstream circuitry during testing of the propagation delay.

22. (Currently Amended) The method as defined in claim 21, further comprising the step of supplying a test enable signal to start testing of the propagation delay.

23. (Previously Presented) The method as defined in claim 18, wherein the arithmetic core is a One-Hot Residue Number System (OHRNS) modulo m adder.

24. (Previously Presented) The method as defined in claim 18, wherein the arithmetic core of the arithmetic circuit is a One-Hot Residue Number System (OHRNS) modulo m multiplier.

25. (New) The arithmetic circuit as defined in claim 1, wherein the output of the arithmetic core is not fed back to any of the inputs of the arithmetic core during normal operation of the arithmetic circuit.

26. (New) The arithmetic circuit as defined in claim 1, wherein the output of the arithmetic core is latched during normal operation of the arithmetic circuit.